Roll No. | | | | | | | | | | | | | Total No. of Pages : 02

Total No. of Questions : 09

B.Tech.(Electronics & Computer Engg.) (2019 Onwards) (Sem.–6)

DIGITAL SYSTEM DESIGN

Subject Code : BTEL-606

M.Code : 71162

Time : 3 Hrs. Max. Marks : 60

INSTRUCTION TO CANDIDATES :

1. SECTION-A is COMPULSORY consisting of TEN questions carrying TWO marks each.
2. SECTION-B contains FIVE questions carrying FIVE marks each and students have to attempt any FOUR questions.
3. SECTION-C contains THREE questions carrying TEN marks each and students have to attempt any TWO questions.

SECTION-A

Q1. Answer briefly :

a) What is operator used in VHDL?

b) Convert the expression in maxterm $F = (\bar{A} + \bar{B} + \bar{C})(\bar{A} + B + C)(\bar{A} + \bar{B} + C)$

c) What do you mean by ROM?

d) Write the applications of shift registers.

e) Convert $(734)_{10}$ to hexadecimal.

f) Implement the function $F = \bar{A}\bar{B}\bar{C} + \bar{A}B$

g) Differentiate between PLA and PAL.

h) What is the function of a decoder?

i) Using a 8:1 MUX, realize the function $F = m(0,1,5,6,7)$

j) Define FPGA.

SECTION-B

Q2. Convert a T flip-flop to a D flip-flop.

Q3. Compare asynchronous and synchronous counters.

Q4. Explain entity and architecture with reference to VHDL code of full adder circuit.

Q5. Explain hazards in combinational and sequential circuit with example.

Q6. Explain the terms like state, present state, next state, state diagram and state table.

SECTION-C

Q7. Design the sequential detector circuit using FSM to detect a sequence 1100.

Q8. Reduce the following expressions by using K-map and implement the reduced expression by using universal gates only

$$F = (\bar{A}+\bar{B}+\bar{D}).(\bar{A}+C+\bar{D}).(\bar{A}+\bar{B}+C+\bar{D}).(A+B+\bar{D})+(C+\bar{D})$$

Q9. Write short note on following :

a) VHDL

b) Difference of ROM and PLA

c) Data flow

NOTE : Disclosure of identity by writing mobile number or making passing request on any page of Answer sheet will lead to UMC against the Student.